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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,357	12/08/2003	Sang-Hyun Oh	51876P413	4364

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,357	OH ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/731,357. Currently, claims 1-12 are pending.

Specification

2. The specification is objected to as failing to provide support for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). The specification does not provide support for "forming a dielectric layer on exposed surfaces of the first bottom electrode" as recited in claim 1, lines 18-19. Correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. *Claims 1-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (US 5,786,259) in view of Kang (US 5,834,357).*

Kang (pat '259) discloses a method for manufacturing a ferroelectric random access memory (FeRAM) capacitor (figs. 10-17 and accompanying text). The method comprises the steps of: preparing an active matrix obtained by a predetermined process, the active matrix including a semiconductor substrate 201, a transistor, a bit line 207, an ILD 209 which corresponds to the second

ILD of the claimed invention, and a storage node 211 (figs. 10-11 and col. 5, lines 36-57); forming a first bottom electrode 213 on the second ILD 209 and the storage node 211 (fig. 13 and col. 5, lines 58-64); forming another ILD 219, which corresponds to the third ILD of the claimed invention, on exposed surfaces of the first bottom electrode 213 and the second ILD 209 (fig. 14 and col. 6, lines 23-32); planarizing the third ILD 219 until a top face of the first bottom electrode is exposed (fig. 15 and col. 6, lines 32-34); forming a second bottom electrode 215 on the top face of the first bottom electrode 213 (fig. 13 and col. 5, lines 58-64); forming a dielectric layer 221 on exposed surfaces of the second bottom electrode 215 and the third ILD 219 (fig. 16 and col. 6, lines 50-56); and forming top electrode 223 on the dielectric layer (fig. 17 and col. 6, lines 57-60).

The third ILD 219 is planarized using either a chemical mechanical polishing (CMP) method, *as recited in claim 2*, or a blanket etch method, as *recited in claim 3* (col. 6, lines 32-34).

Kang (pat '259) discloses using iridium (Ir) as the material for the first bottom electrode 213, *as recited in claim 4* (col. 6, lines 1-7).

The second bottom electrode employs a material selected from the group consisting of platinum (Pt), iridium (Ir), iridium oxide (IrOx), ruthenium (Ru), rhenium (Re), rhodium (Rh), tungsten (W), titanium (Ti) and a combination thereof, *as recited in claim 5* (col. 6, lines 7- 13).

The dielectric layer 221 uses a ferroelectric material selected from the group consisting of strontium bismuth tantalite ($SrBi_2Ta_2O_9$, SBT), lanthanum (La)-modified bismuth titanate ($(Bi,La)_4Ti_3O_{12}$, BLT) and lead zirconium titanate ($(Pb,Zr)TiO_3$, PZT), neodymium (Nd)-modified bismuth titanate ($(Bi,Nd)_4Ti_3O_{12}$, BNdT) and vanadium (V)-modified bismuth titanate ($(Bi,V)_4Ti_3O_{12}$, BVT), *as recited in claim 6* (col. 6, lines 50-56).

The top electrode 223 employs a material selected from the group consisting of Ir, IrO_x, Ru, Re, Rh, W, Ti and a combination thereof, *as recited in claim 9* (col. 6, lines 60-65).

Kang (pat '259) lacks anticipation in not teaching the steps of: forming a first ILD, as recited in claim1; and forming conductive oxides on exposed sidewalls of the first bottom electrode by carrying out an oxidation process, as recited in claim 1. Kang ('357) discloses a method for forming a capacitor in a memory device (figs. 2-8 and accompanying text). The method comprises forming a semiconductor substrate 50, the substrate having formed thereon a transistor, a bit line 62, a storage node 68, a first ILD 58, and a second ILD 66 (fig. 2 and col. 5, lines 21-44).

The method further comprises forming a bottom capacitor electrode (figs. 4-7 and col. 5, line 49 - col. 6, line 34). In forming the bottom electrode, alternating layers of metal oxide 72a, 72b, 72c and metal 74a, 74b are deposited on the substrate (fig. 4 and col. 5, lines 48-62). In a subsequent processing step, layers of conductive oxide are formed on exposed sidewalls of

the metal layers 74a, 74b via a thermal oxidation process (fig. 7 and col. 6, lines 22-30). Since the metal layers are formed of ruthenium, the layers of conductive oxide formed on the exposed sidewalls of the metal layers are ruthenium oxide layers (col. 6, lines 22-30).

Whereas Kang (pat '357) describes using ruthenium as the material for metal layers 74a, 74b, another embodiment uses iridium in place of ruthenium as the material for metal layers 74a, 74b (col. 6, lines 19-22). So, it follows that when iridium is used in place of ruthenium as the material for the metal layers 74a, 74b, the resulting layers of conductive oxide formed on the sidewalls of the metal layers are iridium oxide layers.

Since both patents are from the same field of endeavor, the purpose for which Kang (pat '357) is relied upon would have been recognized in the pertinent reference of Kang (pat '259) by one of ordinary skill in the art at the time the invention was made.

As discussed above, with respect to claim 4, Kang (pat '259) discloses using iridium as the material for the first bottom electrode 213. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Kang (pat '259) in view of Kang (pat '357) by forming layers of iridium oxide on exposed sidewalls of the first bottom electrode 213 of iridium, as taught by Kang (pat '357), because: unlike insulating oxide, iridium oxide protects the exposed sidewalls of the bottom electrode from exposure to an oxidizing environment during the deposition of the third ILD 219 without

increasing the resistivity of the lower electrode. Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Kang (pat '259) in view of Kang (pat '357) by forming a first ILD prior to forming the second ILD 209, as taught by Kang (pat '357), because: by forming a first ILD prior to forming the second ILD, the transistor gate electrodes 205 are further electrically isolated from the bit line 207 and the storage node 211.

4. *Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang in view of Kang as applied to claim 6 above, and further in view of Paz de Araujo et al. (US 6,080,592).*

As discussed above, with respect to claim 6, Kang (pat '259) discloses forming a dielectric layer 221, which uses a ferroelectric material selected from the group consisting of strontium bismuth tantalite ($SrBi_2Ta_2O_9$, SBT), lanthanum (La)-modified bismuth titanate ($(Bi,La)_4Ti_3O_{12}$, BLT) and lead zirconium titanate ($(Pb,Zr)TiO_3$, PZT), neodymium (Nd)-modified bismuth titanate ($(Bi,Nd)_4Ti_3O_{12}$, BNdT) and vanadium (V)-modified bismuth titanate ($(Bi,V)_4Ti_3O_{12}$, BVT) (col. 6, lines 50-56). While Kang (pat '259) discloses using a ferroelectric material as the material for the dielectric layer 221, Kang (pat '259) does not teach that the ferroelectric material has a perovskite crystal structure, *as recited in claim 7*; or that the ferroelectric material has a layered perovskite crystal structure, *as recited in claim 8.*

The Paz de Araujo et al. patent (Araujo) discloses a method for forming a ferroelectric material that has a layered perovskite crystal structure (col. 6, lines 17-44). Araujo teaches that ferroelectric materials with layered perovskite crystal structures have less degradation and fatigue (Araujo - col. 5, lines 8-25; col. 5, lines 40-62; and col. 6, lines 5-14)

Since Kang (pat '259) and Araujo are from the same field of endeavor, the purpose for which Araujo is relied upon would have been recognized in the pertinent reference of Kang (pat '259) by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Kang (pat '259) and Kang (pat ' 357) in view of Araujo by forming the dielectric layer 221 of a ferroelectric material, which has a layered perovskite crystal structure, as taught by Araujo, because ferroelectric materials with layered perovskite crystal structures have less degradation and fatigue.

5. *Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (pat '259) in view of Kang (pat '357) as applied to claim 1 above, and further in view of Moise et al. (US 6,211,035 B1).*

Kang (pat '357) does not teach that the oxidation process for forming the iridium oxide layers is carried out by using a plasma gas, *as recited in claim 10*; or that the oxidation process is carried out by using a plasma gas selected from the group consisting of oxygen (0_2) gas, argon (Ar) gas, nitrogen (N_2) gas,

chlorine (Cl) gas, fluorine (F) gas and a combination thereof at a temperature ranging from a room temperature to about 400°C, *as recited in claim 11.*

The Moise et al. Patent (Moise) teaches forming iridium oxide by carrying out an oxidation process, wherein the oxidation process is carried out by using a plasma gas selected from the group consisting of oxygen (O_2) gas, argon (Ar) gas, nitrogen (N_2) gas, chlorine (Cl) gas, fluorine (F) gas and a combination thereof at a temperature ranging from a room temperature to about 400°C (col. 13, lines 32-48).

Since Kang (pat '357) and Moise are from the same field of endeavor, the purpose for which Moise is relied upon would have been recognized in the pertinent reference of Kang (pat '357) by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Kang (pat '259) and Kang (pat ' 357) in view of Moise by carrying out the oxidation process using a plasma gas, as taught by Moise, because: iridium oxide layers formed by plasma oxidation appear to have smoother surfaces than those formed by furnace oxidation, and at a much lower temperature (Moise - col. 13, lines 59-61).

6. *Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (pat '259) in view of Kang (pat '357) as applied to claim1 above, and further in view of Sato (US 5,030,331).*

While Kang (pat '357) discloses forming the iridium oxide by carrying out the oxidation process via an annealing process (col. 6, lines 22-30), Kang does not teach that the annealing process is performed in an ambient of a gas selected from the group consisting of 0_2, N_2 and a combination thereof, at a temperature ranging from about 200°C to about 600°C, *as recited in claim 12.*

Sato teaches forming iridium oxide by carrying out an oxidation process via an annealing process, wherein the annealing process is performed in an ambient of a gas selected from the group consisting of 0_2, N_2 and a combination thereof, at a temperature ranging from about 200°C to about 600°C (col. 3, lines 3-11).

Since Kang (pat '357) and Sato are from the same field of endeavor, the purpose for which Sato is relied upon would have been recognized in the pertinent reference of Kang (pat '357) by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Kang (pat '259) and Kang (pat ' 357) in view of Sato by carrying out the oxidation process using an annealing process, as taught by Sato, because: the resulting iridium oxide is of good quality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
29 September 2004

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